REMARKS

Applicants respectfully request reconsideration of the instant application in view of the foregoing amendments and the following remarks.

Claim Rejections – 35 U.S.C. § 103

Claims 1, 2, 4, and 12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Number 6,288,431 ("Iwasa") in view of U.S. Patent Number 4,996,574 ("Shirasaki") and U.S. Patent Number 4,356,211 ("Riseman"). Claim 3 was rejected under § 103(a) as being unpatentable over Iwasa in view of Shirasaki and Riseman and further in view of U.S. Patent Number 4,868,632 ("Hayashi"). Applicants respectfully traverse these rejections for at least the following reasons.

With respect to claim 1, Applicants respectfully submit that the proposed combination of Iwasa, Shirasaki, and Riseman, *at a minimum*, fails to describe or suggest a semiconductor device that includes, among other features, a channel stopper formed in a region located at a bottom portion of the trench in the semiconductor substrate and containing an impurity of the first conductive type at a higher concentration than that in the semiconductor substrate, wherein the channel stopper is formed ***under*** the semiconductor FIN.

The Office Action concedes that Iwasa in view of Shirasaki do not appear to describe this feature. Office Action at page 3. The Office Action, however, asserts that Riseman provides such a teaching and further asserts that it would have been obvious to modify Iwasa in view of Shirasaki to have a channel stopper formed in a region located at a bottom portion of the trench in the semiconductor substrate. Office Action at pages 3, 4. Applicants disagree.

Riseman relates to a technique for electrically isolating devices from one another, where

a plurality of trenches is formed inside a single substrate. *See* Riseman at Abstract. To illustrate, referring to FIG. 4, Riseman describes forming trenches 20 inside a substrate 10. *See* Riseman at col. 4, lines 14-20. After trenches 20 are formed, a channel stopper 22 is formed by injecting boron (B) into a bottom part of each of the trenches 20. *Id.* Thereafter, as shown in FIG. 5 of Riseman, a silicon dioxide film is formed on the channel stopper 22. *See* Riseman at col. 4, lines 23-31.

Although Riseman appears to describe a channel stopper, it does not describe that the alleged channel stopper is formed ***under*** a semiconductor FIN. In contrast, Riseman describes that the channel stopper is formed under an isolation region for isolating devices from one another. As such, Riseman does not describe or suggest a semiconductor device that includes, among other features, a channel stopper formed in a region located at a bottom portion of the trench in the semiconductor substrate and containing an impurity of the first conductive type at a higher concentration than that in the semiconductor substrate, wherein the channel stopper is formed ***under*** the semiconductor FIN.

The Office Action asserts that it would have been obvious to modify Iwasa in view of Shirasaki to have a channel stopper, as taught by Riseman, formed in a region located at a bottom portion of the trench in the semiconductor subscriber. Office Action at pages 3, 4. Although Riseman teaches that a channel stopper 22 is formed beneath a bottom wall 23 of each of trenches 23, Applicants do not agree with the Office Action that Iwasa and Shirasaki can be modified to include a channel stopper region as recited in claim 1.

To illustrate, referring to FIGS. 1 and 3D, Iwasa shows a MOS transistor that includes a pillar projection 11 and a gate electrode 21. Iwasa at col. 11, lines 50-57. The pillar projection 11 serves as an active region and is formed on the surface of substrate 1. *Id.* The gate electrode

21 covers the pillar projection 11. Iwasa at col. 11, lines 59-60. In this MOS transistor, as shown by FIGS. 2A-2D, the pillar projection 11 is formed by the removal of the substrate 1.

As such, one of ordinary skill in the art would understand that it would not be possible to modify Iwasa to include a channel stopper, as taught by Riseman, under the semiconductor FIN. The channel stopper taught by Riseman is formed via an ion implantation. However, the pillar projection 11 of the Iwasa would act as a barrier and would prevent formation of such a channel stopper beneath the pillar projection 11. As such, Iwasa cannot be combined with Riseman to describe a channel stopper formed in a region located at a bottom portion of the trench in the semiconductor substrate and containing an impurity of the first conductive type at a higher concentration than that in the semiconductor substrate, wherein the channel stopper is formed ***under*** the semiconductor FIN, as recited in claim 1.

Notwithstanding the above and even assuming for the sake of argument that it is possible to combine the semiconductor FIN of Iwasa with the channel stopper of Riseman to form a channel stopper below the semiconductor FIN, the proposed combination still fails to render claim 1 obvious. As amended, claim 1 recites that the semiconductor FIN is formed ***after*** forming the channel stopper. However, the proposed combination of the cited prior art requires formation of the semiconductor FIN ***before*** the formation of the channel stopper. That is, the proposed combination of Iwasa and Riseman, requires first forming the semiconductor FIN by etching the substrate and then forming the channel stopper by ion implementation of Riseman.

Similar to Iwasa, Shirasaki also describes forming a silicon plate 31 by cutting into the substrate 32. In particular, referring to FIG. 10, Shirasaki describes that "a pit 30 is formed in a silicon substrate 32 except for a part corresponding to a silicon plate 31. In other words, the silicon plate 31 extends upwardly from the bottom of the pit 30." Shirasaki at col. 7, lines 35-40.

As such, for the same reasons presented above, it appears to be impossible to modify Shirasaki to include a channel stopper under the silicon plate 31. Furthermore, the proposed combination of Shirasaki and Riseman fails to describe or suggest that the semiconductor FIN is formed ***after*** forming the channel stopper, as recited in amended claim 1.

For at least the foregoing reasons, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 1, along with its dependent claims.

Claims 6, 8, and 13 were rejected under § 103(a) as being unpatentable over Iwasa in view of Shirasaki and Riseman and further in view of U.S. Patent Number 7,163,851 ("Abadeer"). Claim 7 was rejected under § 103(a) as being unpatentable over Iwasa in view of Shirasaki, Riseman, Abadeer, and Hayashi. Applicants traverse these rejections for at least the following reasons.

Claim 6 recites a semiconductor device that includes, among other features, a first field-effect transistor including a semiconductor substrate in which a trench is formed and containing an impurity of a first conductive type, a first source region and a first drain region each of which is buried in the trench and contains an impurity of a second conductive type, and a channel stopper formed in a region located at the bottom of the trench in the semiconductor substrate and containing an impurity of the first conductive type at a higher concentration than that in the semiconductor substrate, wherein the semiconductor FIN is formed ***after*** forming the channel stopper, and the channel stopper is formed ***under*** the semiconductor FIN. Therefore, for at least

the reasons presented above with respect to claim 1, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 6, along with its dependent claims.[1]

Claims 14, 16-18, and 20-22 were rejected under § 103(a) as being unpatentable over Iwasa in view of Riseman. Claim 15 was rejected under § 103(a) as being unpatentable over Iwasa in view of Riseman and further in view of US. Patent Number 6,770,516 ("Wu"). Claim 19 was rejected under § 103(a) as being unpatentable over Iwasa in view of Riseman and Shirasaki. Applicants traverse these rejections for at least the following reasons.

Claim 14 recites a semiconductor device that includes, among other features, a heavily doped impurity region of the conductive type formed in the semiconductor region at the bottom portion of the trench and under the semiconductor FIN and the source and drain regions, wherein the semiconductor FIN is formed ***after*** forming the heavily doped impurity region, and the heavily doped impurity region is formed ***under*** the semiconductor FIN. Therefore, for at least the reasons presented above with respect to claim 1, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 14, along with its dependent claims.

Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Therefore, it is respectfully requested that the rejection under § 103 be withdrawn.

Conclusion

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If

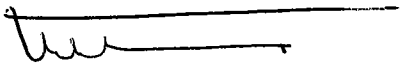
[1] Abadeer was relied upon for an alleged teaching of forming two field-effect transistors on the same substrate. As such, Applicants do not believe that the proposed addition of subject matter from Abadeer remedies the shortcomings of Iwasa, Shirasaki, and Riseman to describe or suggest the above-recited features of claim 6.

there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



Babak Akhlaghi
Limited Recognition No. L0250

Please recognize our Customer No. 53080 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 BA:blb
Facsimile: 202.756.8087
Date: October 7, 2009